REMARKS

Claims 1, 3, 5-12, 14, 15, 18, 20, 24-27 and 32-35 are pending in the application.

Claims 1, 3, 5-12, 14, 15, 18, 20, 24-27 and 32-35 are rejected.

Claims 1, 6, 7 and 24-27 stand rejected under 35 U.S.C. § 103(a).

Claims 10, 12, 14, 15, 18 and 20 stand rejected under 35 U.S.C. § 103(a).

Claims 32-35 stand rejected under 35 U.S.C. § 103(a).

Claims 10 and 12 have been amended.

Claims 36-38 have been added.

No new subject matter has been added.

The Applicant respectfully requests reconsideration of claims 1, 3, 5-12, 14, 15, 18, 20, 24-27 and 32-38 in light of the following amendment and remarks.

Claim Rejections – 35 U.S.C. § 103

Claims 1, 6, 7 and 24-27 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Deering (U.S. Pat. No. 5,544,306), hereinafter "Deering," Baldwin (U.S. Patent No. 5,727,192 A), hereinafter "Baldwin," and Shiraishi (U.S. Pat. No. 5,828,378), hereinafter "Shiraishi."

Claims 3, 5, 8, 9 and 11 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Deering, Baldwin, and Shiraishi, in view of Dowdell (U.S. Pat. No. 5,301,263), hereinafter "Dowdell."

Claims 10, 12, 14, 15, 18 and 20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Deering and Shiraishi, in view of Dowdell and Diefendorff (US Patent No. 5,268,995), hereinafter "Diefendorff."

Claims 32-35 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ryherd (U.S. Pat. No. 4,970,499), hereinafter "Ryherd," and Dowdell.

The Applicant respectfully traverses the rejections.

Claim 15 sets forth the method of claim 12, wherein "writing the external depth data takes place if the comparison yields that the external depth data is larger than the internal depth data." Support for this claim can be found at, for example, page 5, lines 28-31 of the present application as originally filed.

The Examiner contends that Dowdell teaches the features set forth in claim 15 because "Dowdell teaches bytes R1, R2, and R3 of old z-values and W1, W2, and W3 of new z-values (c.

4, ll. 34-50) and comparison is performed between R1 and W1 and if R1>W1, then it is determined old z-value is greater than new z-value and consequently new z-value is written to memory 124 (c. 5, ll. 5-10)." Office Action dated July 14, 2008, pages 14-15, section 24. However, upon closer inspection, Dowdell teaches precisely the opposite of what is recited in claim 15. Consider, for example, that the Office Action proposes that bytes R1, R2, and R3 are equivalent to the old z-values (the alleged internal depth data) and that bytes W1, W2, and W3 are equivalent to the new z-values (the alleged external depth data). Office Action dated July 14, 2008, page 14, section 24. But, Dowdell clearly teaches that if the R1 value (the old z-value) is greater than W1 (the new z-value), then consequently the new z-value is written to memory 124. Dowdell, column 5, lines 5-10 and Office Action, page 15, section 24. Indeed, Dowdell does not teach that if the external depth data is larger than the internal depth data, writing the external depth data, as set forth in claim 15 (and as set forth in independent claim 12, from which claim 15 depends). Dowdell's disclosure actually teaches away from the very notion by stating:

> . . . if R1<=W1, then the old 24 bit z-value is less than the new 24 bit z-value, indicating that the new value should not be written to the memory. In this case, the updating operation is terminated immediately as indicated by the "done" state of FIG. 2.
> [Dowdell, column 5, lines 10-14]

In view of the above, Dowdell fails to teach the limitations of method claim 15. Deering, Shiraishi, and Diefendorff fail to remedy the deficiencies of Dowdell at least in this respect. Therefore, the Applicant respectfully submits that claim 15 is patentable under 35 U.S.C. 103(a) over Dowdell, even when viewed with Deering, Shiraishi and Diefendorff, and is therefore allowable.

Claim 35 sets forth "wherein at least one status signal is transmitted from the memory device to the memory controller, the at least one status signal indicating whether the internal depth data was replaced with the external depth data, the at least one status signal being transmitted responsive to one of the sixth and the seventh of the seven clock cycles." Support for this claim can be found at, for example, FIG. 4 and the associated detailed description of the present application as originally filed.

Nowhere do Dowdell and Ryherd disclose at least one status signal being transmitted responsive to one of the sixth and the seventh of the seven clock cycles, as set forth in claim 35. The Examiner proposes that the INVALID bit of Dowdell is the at least one status signal of the claims. However, the INVALID bit indicates whether to write the new z-value to memory, and

nowhere does Dowdell ever mention or suggest that the INVALID bit is a status signal or provides status that the internal depth data was replaced with the external depth data, as set forth in claim 35. For example, Dowdell states "the controller 122 (FIG. 1) begins by checking the value of the INVALID bit for the given pixel and, depending on its value, either writing the new z-value to memory or initiating the update process described in the state diagram of FIG. 2." Dowdell, column 8, lines 25-31. The REPLACED bit stored in the CENTRAL FIFO 312 of Dowdell (FIG. 3) appears to be more akin to a status signal, which indicates a '1' if a replacement of the z-value occurred and '0' if one did not. Dowdell, column 8, lines 36-39. However, because the scheme disclosed in Dowdell "yields out-of-order completion . . . the z-value updating for pixels does not necessarily occur in the same order in which information for the pixels appeared in the stream . . . ." Dowdell, column 8, lines 40-43. Dowdell explains the out-of-order processing in detail, as follows:

> Note that this scheme, in general, yields out-of-order completion. That is, the z-value updating for pixels does not necessarily occur in the same order in which the information for the pixels appeared in the stream as received by the assignment unit 304. For example, this phenomenon would occur if a large percentage of the pixels arriving at the assignment unit had addresses such that they were to be assigned to a particular one of the processor modules 100. In this case, a lengthy queue would form at this processor, and pixels arriving at the assignment unit later but which corresponded to other processing modules would be updated before those pixels queued at the crowded processor. Further, pixels processed by certain processors may result in quicker "done" states. Permitting out-of-order completion clearly avoids the possibility of forming queues at all processors when queues have formed at a few busy processors and consequently allows the eight processor parallelism to be fully exploited.
> [Dowdell, column 8, lines 40-58]

In view of the above, there is no certainty or guarantee of when the z-value updating will occur in the status information stored in CENTRAL FIFO 312 of FIG. 3. In view of the above, there is no timing guarantee that z-values will have their status updated within any certain period of time or number of clock cycles because "z-value updating for pixels does not necessarily occur in the same order in which the information for the pixels appeared in the stream received by the assignment unit 304." While the INVALID bit may arguably be processed around the time of the read/compare/write operation (as suggested in the Office Action at page 17, section 27), the INVALID bit is not a status bit indicating whether the internal depth data was replaced with the external depth data, as explained above, but rather the INVALID bit indicates whether to write the new z-value to memory.

Moreover, Ryherd never mentions or suggests a status signal. While Ryherd discloses a graphical representation of the operation of the local display processor in terms of the utilization of clock cycles (column 3, lines 11-14), the graphical representation is directed toward "pipelining operations" which allows read, compare, and conditional write operations to be performed during a single clock cycle. Ryherd, FIG. 6 and column 6, lines 5-11. The Examiner states "So, device of Ryherd can be modified to include the status signal of Dowdell to be transmitted responsive to one of sixth and seventh of seven clock cycles." Office Action, page 18, section 30. The Examiner states the reasons this would be obvious by referring to the reasons given with claim 32, those reasons stating that "Dowdell suggests this is needed so memory controller knows when internal depth data was replaced with external depth data so memory controller knows when to retrieve new external depth data to send to processor for processing (c. 8, ll. 12-39)." Office Action, page 17, section 27. However, column 8, lines 12-39 of Dowdell states the following:

> The processing module number is accompanied on the central FIFO by two single-bit state variables: REPLACED and DECISION-COMPLETE. These two variables indicate whether or not the new z-value has replaced the old z-value in the entry to which they correspond and whether or not this decision has been made, respectively. DECISION-COMPLETE is initialized to `0`, and as long as DECISION-COMPLETE remains `0`, the value of REPLACED is meaningless.
>
> As an entry emerges from the input FIFO 102 belonging to its processing module 100, the processing module initiates the read/compare/write operation described in Section I above. Specifically, the controller 122 (FIG. 1) begins by checking the value of the INVALID bit for the given pixel and, depending on its value, either writing the new z-value to memory or initiating the update process described by the state diagram of FIG. 2. At this point, the old z-value either has or has not been replaced by the new z-value, and an indication to that effect is provided to the central FIFO 312. In particular, the oldest entry in the central FIFO 312 corresponding to the current processing module 100 is updated by setting the value of the single bit REPLACED to `1` if a replacement occurred and `0` if one did not. Simultaneously, the value of DECISION-COMPLETE is set to `1`.
> [Dowdell, column 8, lines 12-39]

The excerpted language from Dowdell, as cited in the Office Action at page 17, section 27, and reproduced above, does not teach or suggest "so memory controller knows when internal depth data was replaced with external depth data so memory controller knows when to retrieve new external depth data to send to processor for processing." Rather, the excerpted language

describes the role of the REPLACED bit in indicating whether or not the new z-value has replaced the old z-value. Shortly thereafter (at column 8, lines 40-58), Dowdell explains how the status is updated in an out-of-order scheme. Suppose that Dowdell were modified such that the status got updated responsive to the sixth clock signal of Ryherd as shown in FIG. 6. The entire out-of-order updating scheme would be rendered inoperable for its intended purpose because by imposing a fixed period of time for completion, the out-of-order processing would fail.

Even if Dowdell somehow disclosed that the invention illustrated in FIGs. 2 and 3 of Dowdell could accomplish issuing status signals responsive to the sixth clock cycle relative to the "pipelining operations" which allows read, compare, and conditional write operations to be performed during a single clock cycle (the pipelining operations of which are shown in FIG. 6 of Ryherd), such a disclosure does not—by itself—objectively establish that the memory controller would therefore know when to retrieve new external depth data to send to the processor for processing simply by modifying the teachings of Dowdell using Ryherd as proposed.

The Office Action fails to identify any basis in fact or technical reasoning reasonably supporting a determination that: (a) the invention illustrated in FIGs. 2 and 3 of Dowdell must necessarily issue status signals responsive to the sixth clock cycle using Ryherd as proposed; or (b) that the memory controller can know when to retrieve new external depth data to send to the processor for processing only if the status signals are issued responsive to the sixth clock cycle using Ryherd as proposed. In view of the above, and absent any objective evidence to the contrary, the Office Action fails to objectively establish that one of ordinary skill in the art actually would modify Dowdell using Ryherd "so memory controller knows when internal depth data was replaced with external depth data so memory controller knows when to retrieve new external depth data to send to processor for processing." Thus, the Applicant respectfully submits that claim 35 is patentable under 35 U.S.C. 103(a) over Ryherd and Dowdell, and is therefore allowable.

Regarding claim 32, the Examiner states that: "If it is determined that new z-value should not be written to memory and should not overwrite old z-value, then "done" state is entered, then INVALID bit is set to 0 in memory controller (122) to indicate that updating operation is completed when "done" state has been reached and new z-value was not written to memory (c. 5, ll 38-41, 46-48; c. 3, ll. 42-51)." Office Action, page 16, section 27. The Examiner further concludes that the INVALID bit indicates "whether internal (old) depth data was replaced with external (new) depth data" because "INVALID bit = '1' if was replaced, INVALID bit = '0' if

was not replaced . . . ." Office Action, top of page 17. However, the Applicant respectfully submits that the Examiner has mis-ordered the steps and processes that are disclosed in Dowdell, and therefore draws an incorrect conclusion based on the mis-ordering of the steps.

For example, the z-value updating operation proceeds to completion in one of two ways depending on the value of the INVALID bit. The INVALID bit itself does not give status of whether the old depth data was actually replaced with the new depth data, nor is the INVALID bit set to '1' or '0' to indicate that the operation is completed. Indeed, it is the REPLACED bit and the DECISION_COMPLETE bit that perform the function of giving status of whether the old depth data is replaced with the new depth data. Dowdell, column 8, lines 12-18; column 5, lines 42-54. Further, Dowdell explicitly teaches away from the limitation of claim 32, which sets forth "the at least one status signal being transmitted responsive to a predetermined number of clock cycles," because as previously explained, Dowdell discloses an on out-of-order completion scheme, which depends on queue depth of processors rather than a predetermined number of clock cycles. Dowdell, column 8, lines 40-58. Therefore, a person having skill in the art would not have been motivated to combine the out-of-order status completion of Dowdell with the pipelined processor of Ryherd. For at least these reasons, the Applicant submits that claim 32 is patentable under 35 U.S.C. 103(a), and is allowable, as are dependent claims 33 and 34.

Regarding claim 1, for substantially the reasons explained with reference to claim 32, the Applicant respectfully submits that the cited references fail to teach "output to the memory controller a status signal within predetermined clock cycles from receipt of the activate command from the memory controller," as set forth in claim 1. Thus, claim 1 is patentable under 35 U.S.C. 103(a), and is in proper form for allowance. Based at least on their dependency from claim 1, and for their own merits, claims 3, 5-9 and 24-27 are likewise in allowable form.

Regarding claims 10 and 12, the Examiner suggests that the least significant bit b0 of Diefendorff is the first status signal indicating that the lower X bits of the internal depth data have been modified and that second bit b1 of Diefendorff is the second status signal indicating that the upper X bits of the internal depth data have been modified, as set forth in claims 10 and 12. However, the least significant bit b0 and the second bit b1 of Diefendorff are not status signals, but rather, bit b0 "indicates that the least significant pixel (and Z-value) needs to be stored, but not the most significant pixel" and bit b1 "indicates that the most significant pixel needs to be stored, but not the least significant pixel." Diefendorff, column 8, lines 28-34. The bit b0 says nothing about whether the least significant pixel was actually stored—only that needs

to be. And the bit b1 says nothing about whether the most significant pixel was actually stored—only that it needs to be. Further, the limitations of claim 10 and 12 are not directed toward whether a least significant pixel or most significant pixel need to or were actually stored. Rather, claims 10 and 12 are directed toward status signals indicating whether the lower or upper X bits of the z-value itself were modified. Nor are the least significant bit b0 or second bit b1 status signals indicating whether the upper or lower bits of the internal depth data have been modified.

Nevertheless, in order to clarify their scope, claims 10 and 12 have been amended to set forth "a first status signal indicating that the lower X bits of the internal depth data have been over-written with the external depth data" and "a second status signal indicating that the upper X bits of the internal depth data have been over-written with the external depth data."

In contrast, the INVALID bit of Dowdell merely indicates "whether or not the corresponding z-value memory location has a valid z-value stored in it," not whether it has been over-written with the external depth data. Dowdell, column 4, lines 6-9. Further, for the reasons explained above, Diefendorff fails to remedy the deficiencies of Dowdell in this respect. Deering and Shiraishi also fail to teach each of the limitations of amended claims 10 and 12, whether viewed individually or in combination with Dowdell and Diefendorff. Thus, the Applicant respectfully submits that claims 10 and 12 are patentable under 35 U.S.C. 103(a), and are therefore allowable, as are dependent claims 11, 14, 15, 18 and 20.

New Claims

New claim 36 depends from claim 6 and generally corresponds to the limitations of claim 15. For substantially the reasons given above with reference to claim 15, the Applicant respectfully submits that claim 36 is in proper form for allowance.

New claim 37 depends from claim 32 and generally corresponds to the limitations of claim 33, although setting forth "if the external depth data is larger than the internal depth data" rather than "if the external depth data is smaller than the internal depth data." For substantially the reasons given above with reference to claim 15, the Applicant respectfully submits that claim 37 is in proper form for allowance.

New claim 38 depends from claim 10 and generally corresponds to the limitations of claim 15. For substantially the reasons given above with reference to claim 15, the Applicant respectfully submits that claim 38 is in proper form for allowance.

For the foregoing reasons, reconsideration and allowance of claims 1, 3, 5-12, 14, 15, 18, 20, 24-27 and 32-38 of the application as amended is requested. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

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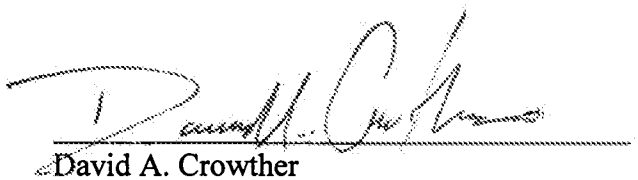

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